9.1 A Wide Power-Supply Range (0.5V-to-1.3V) Wide Tuning Range (500 MHz-to-8 GHz) All-Static CMOS AD PLL in 65nm SOI

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A recurring issue in porting digital designs to new technologies is remapping the analog circuits that are necessary to make digital circuits work. In this paper, we present an all-static CMOS all-digital PLL (ADPLL) designed exclusively with standard cells—except for the tri-state inverter in the digitally-controlled oscillator (DCO), which required custom layout —that can be remapped just like any other digital circuit.

Figure 9.1.1 shows the top-level architecture of the ADPLL [1-3]. A bang-bang phase and frequency detector (PFD) generates one bit of phase difference information. This bit is passed through a proportional-differential-integral (PDI) digital filter to generate control signals for a DCO. The output of the DCO is finally divided down and compared with a reference at the PFD. The accuracy of the DCO is enhanced using a ΔΣ modulator to dither some of the input control bits.

The DCO, shown in Fig. 9.1.2 consists of tri-state inverters. These tri-state inverters can be turned on one at a time to generate a total of 768 frequency steps. The inverters are arranged in a 17 row × 48 column matrix, where the last row is dedicated to fixed and frequency dithering inverters. The inverters are sized to balance up and down transitions, thus minimizing the impulse sensitivity function of the oscillator [4].

Inverters in each row are turned on or off one at a time. When the row is full, we move to the next row, when the row is empty we move to the previous one. A row control mechanism determines which rows are held fully on, and which is the row that is being affected by the column control. Row overrides can be used to restrict the tuning range, and thus reduce lock time.

The DCO sits on a separate, unregulated power supply V_{DDA}, which is typically set to the same value as the power supply for the rest of the digital circuit. If necessary, level shifting is performed by the control logic sitting next to each inverter.

Two versions of the ADPLL are implemented: one using regular threshold devices (RVT, Vt ≈ 200mV) and one using high-threshold devices (HVT, Vt ≈ 300mV). Figure 9.1.6 shows the HVT DCO tuning curves at power supplies ranging from 0.3 to 1.3V, at 100°C.

The output clock of the DCO is divided down in two stages. The first stage divides by 4 or 8, using static dividers. This clock drives all of the digital logic. The second divider stage receives the output of the first stage and generates a clock gating signal that effectively divides the activity of the clock by an extra factor M=1, 2, 3,…8. This gating signal is used by the loop filter, the row and column control of the DCO, and the PFD.

The loop filter consists of an integral stage, followed by a proportional-differential stage. Proportional, integral, and differential constants are 4 bits and programmable. All arithmetic is done on 5-bit registers. Overflows and underflows are sent to the DCO control as frequency increment/decrement commands, thus avoiding not only arithmetic on longer registers, but also binary to thermometer code conversion, which is implicitly done by the DCO control. The effective precision of the arithmetic is 14.5 bits (5 bits plus 9.5 equivalent bits that control the state of the DCO). The 5-bit output of the filter is fed to a MASH ΔΣ modulator [5]. The modulator can be programmed to be 1st, 2nd, or 3rd order, or turned off altogether. The modulator produces 7 output bits that are used to directly control 7 tri-state inverters in the DCO array. The PFD, shown in Fig. 9.1.3, determines which is the earliest arriving edge using a mutual exclusion element (mutex). The mutex consists of a set-reset latch, followed by a metastability filter. When both outputs of the latch are at least one threshold voltage apart, the filter stage produces an output. This output is stored in a latch that feeds the loop filter. A self-timed circuit [6] verifies that both inputs have arrived and the result has been properly stored, and generates a reset for the edge sensitive input latches. This device detects both frequency and phase.

A duty-cycle correction (DCC) circuit is present at the output of the DCO. This circuit comprises a pair of inverters with programmable pull-up and pull-down strengths, followed by buffers that drive the output clock.

The clock is taken off-chip by differential open drain drivers. These, and the reference clock receiver, are the only non-static-CMOS circuits, and are there only for the purpose of testing the chip.

This design was fabricated in 65nm CMOS SOI. The active area of the circuit is 200×150μm². The PLL operates correctly from 0.5 to 1.3V power supply. At 0.5V, 100°C the PLL locks from 90MHz up to 1.2GHz with a power dissipation of 1.6mW/GHz. At 1.3V, 25°C, the PLL locks from 500MHz to 8GHz, with a power dissipation of 8mW/GHz.

Figure 9.1.4 shows a measured phase noise plot for the closed loop PLL, for 0th, 1st, and 2nd order ΔΣ, with the best result being -112dBc/Hz at 4GHz center frequency 10MHz offset. Some extra improvement is obtained from 3rd order ΔΣ, but it is only marginal and does not justify the power of the extra stage.

For digital circuit clock synthesis applications, a very important figure of merit is the period jitter. Period jitter determines the shortest clock cycle that can be generated by the PLL at a given frequency, which, in turn, drives the timing closure of the digital circuit. At 1.2V/4GHz, we measured a period jitter of 0.7ps_{rms}, and at 0.5V/1GHz, we measured 3.2 ps_{rms}. These numbers compare very well with those obtained from analog PLLs, showing that there is no penalty paid in period jitter because of frequency dithering.

Figure 9.1.5 shows a graph of *N*-cycle jitter accumulation for the closed loop PLL. As expected, the accumulation flattens out as *N* output cycles cover more than one reference input cycle. The overshoot before flattening is due to the latency of the control loop, three reference clock cycles in this design.

References:

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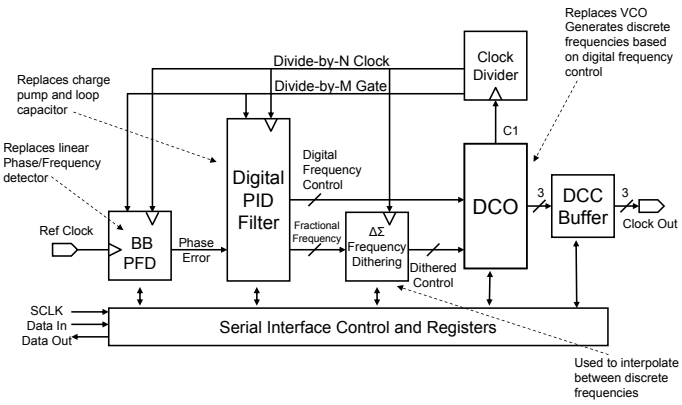


Figure 9.1.1: Top level architecture of the ADPLL.

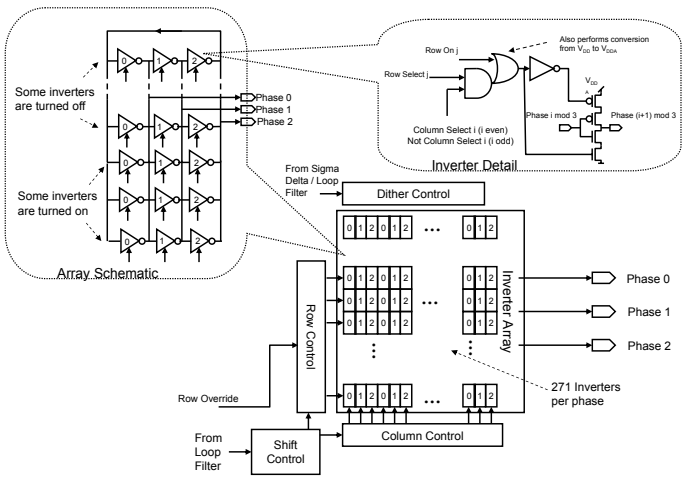


Figure 9.1.2: Schematic of the DCO.

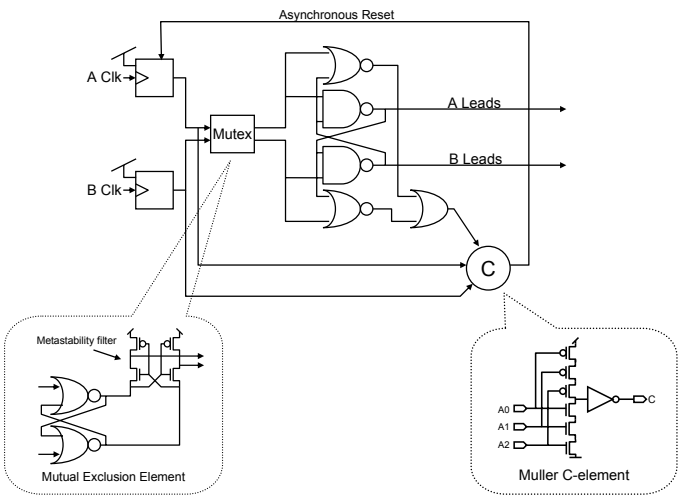
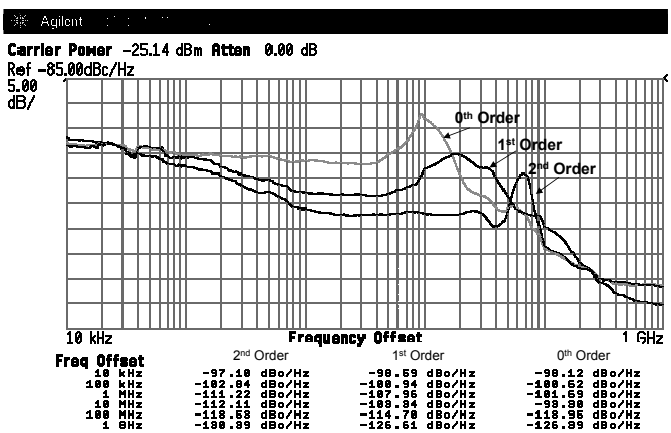


Figure 9.1.3: Self-timed bang-bang PFD.



Freq Offset	2nd Order	1st Order	0th Order
10 kHz	-97.10 dBc/Hz	-98.59 dBc/Hz	-98.12 dBc/Hz
100 kHz	-102.84 dBc/Hz	-100.94 dBc/Hz	-100.62 dBc/Hz
1 MHz	-111.22 dBc/Hz	-107.96 dBc/Hz	-101.69 dBc/Hz
10 MHz	-112.11 dBc/Hz	-108.94 dBc/Hz	-98.98 dBc/Hz
100 MHz	-118.58 dBc/Hz	-114.78 dBc/Hz	-118.96 dBc/Hz
1 GHz	-130.39 dBc/Hz	-126.61 dBc/Hz	-126.39 dBc/Hz

Figure 9.1.4: Phase noise diagram for the locked ADPLL, for 0th, 1st, and 2nd order ΔΣ. Reference frequency is 250MHz, output frequency is 4GHz.

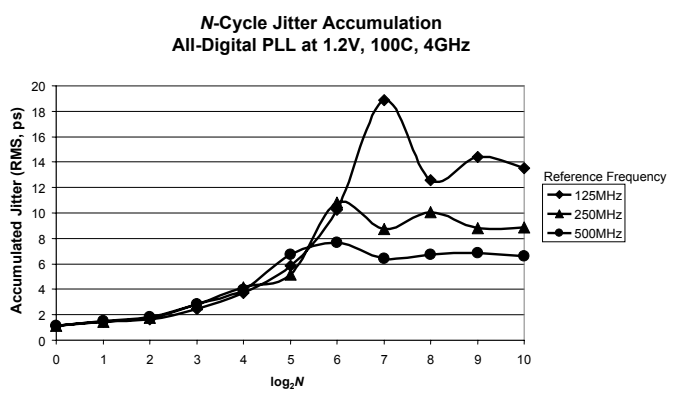


Figure 9.1.5: Jitter accumulation graph for the closed loop ADPLL, with division ratios of 8, 16, and 32.

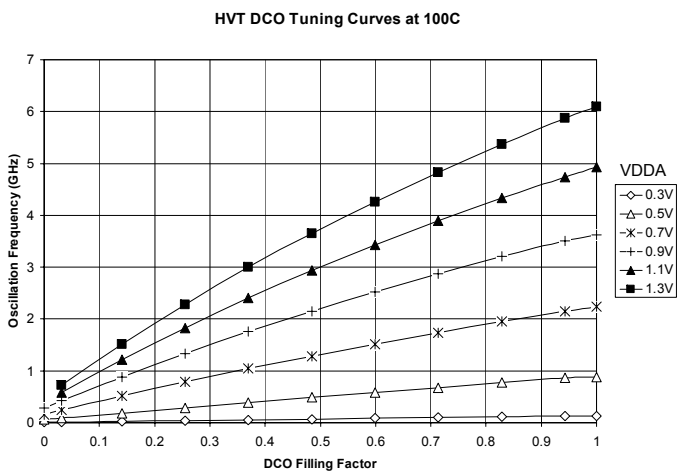


Figure 9.1.6: Measured tuning curves of the HVT DCO at 100°C as a function of the fraction of inverters turned on.

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